SESSION 3 – TAPA III
Advanced High Data Rate DRAMs

Thursday, June 17, 10:20 a.m.
Chairpersons: S. Nataranjan, Mosys
H. Ikeda, Elpida

3.1 — 10:20 a.m.

Burst Cycle Data Compression Schemes for Pre-Fuse Wafer-Level Test in Large Scale High-Speed Embedded DRAM, R. Fukuda, K. Kobayashi, M. Akamatsu*, M. Kaihatsu*, A. Tamura*, K. Taniguchi* and Y. Watanabe, Toshiba Corporation Semiconductor Company, Kanagawa, Japan, *Sony Corporation Semiconductor Solutions Network Company, Tokyo, Japan

This paper describes two novel data compression schemes suitable for high density and high speed embedded DRAMs. The parallel compression serial readout scheme reduces bit-scan test times to one eighth. The parallel compression multiplexed readout scheme realizes high frequency at-speed tests even with lowcost testers. Both can be used for pre-fuse wafer tests requiring redundancy calculations. The new schemes have been implemented in a test chip with a 65nm technology and verified.

3.2 — 10:45 a.m.

A 128Mb Multi Port Media DRAM with Four Independent 4Gb/s Serial Ports, S. Lee, K.-W. Kwon, C. Kim, D. Lee*, J. Shin* and S.-I. Cho, Samsung Electronics Company, Hwasung, Korea, *Silicon Image, Inc., Sunnyvale, CA

This paper proposes a 128-Mb multimedia-specific DRAM having four independent 4Gbps RX-TX serial ports, 16 independent banks and 512b I/O bus. The over-sampling clock/data recovery, boosted column select and data-line redundancy schemes realize high-speed data path. It is fabricated using 1.8V0.10um standard DRAM technology.

3.3 — 11:10 a.m.

A 512Mbit, 3.2Gbps/pin Packet-Based DRAM with Cost-Efficient Clock Generation and Distribution Scheme, Y.-S. Sohn, J.-H. Choi, I.-Y. Chung, H. Chung, C.-K. Kim, G.-S. Byun, D.-W. Kang, W.-K. Park, I.-S. Park, H.-S. Hwang, C.-H. Kim and S.-I.Cho, Samsung Electronics Co., Hwasung, Korea

A 1.8V, 512Mbit Packet-based DRAM with 3.2Gbps/pin was designed for main memory of a game console and graphic application. To have lower power consumption and smaller area in clock generation and distribution, 3-row pad structure with reduced clock loading and PLL with loop zero from voltage offset are used. An analytical equation for estimating the input capacitance of pad with ODT (On-Die Termination) is also presented.

3.4 — 11:35 a.m.

1.8-V 800-Mb/s/pin DDR2 and 2.5-V 400-Mb/s/pin DDR1 Compatibly Designed 1Gb SDRAM with Dual Clock Input Latch Scheme and Hybrid Multi-Oxide Output Buffer, H. Fujisawa, M. Nakamura, Y. Takai, Y. Koshikawa, T. Matano, S. Narui, N. Usuki, C. Dono, S. Miyatake*, M. Morino*, K. Arai*, S. Kubouchi*, I. Fujii*, H. Yoko* and T. Adachi, Elpida Memory, Inc., Kanagawa, Japan, *Hitachi ULSI Systems Corp., Tokyo, Japan

Two circuit techniques of DDR1/DDR2 compatible chip architecture designed for high-speed and high-density DRAMs are presented. The dual clock input latch scheme, which reduces the excessive timing margin for random input commands by using a pair of latch circuits controlled by dual-phase 1-shot clock signals, achieves a 0.9-ns reduction in cycle time. By combining a hybrid multi-oxide output buffer, we developed a 175.3 mm2 1Gb SDRAM which operates as a 800-Mb/s/pin DDR2 or 400-Mb/s/pin DDR1.

Lunch 12:00 p.m.